

Memorandum

To	Distribution	Date	21 December 1976
From	Bob Metcalfe	Location	Palo Alto
Subject	Xerox Wire Functional Specification	Organization	SDD/SD



Filed on: <METCALFE>XWFS.BRAVO

The attached *Xerox Wire Functional Specification* is preliminary. Please comment.

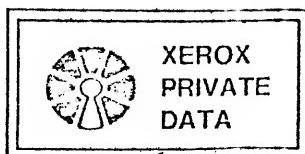
Arrangements tentatively have been made to discuss the contents of this memo with Bo Sramek during the second week of 1977. The purposes of this early EOD interaction are to get design help, particularly on manufacturing and maintenance, and to prepare for our transfer to EOD of engineering models (formerly called breadboards).

What we have here is a snapshot of your various suggestions mashed together by me without attribution. Wider circulation of these specifications should therefore be cautious and coordinated through me.

Distribution

Dave Boggs
Bill Crowther
Butler Lampson
David Liddle
Hal Murray
Brian Rosen
Ed Taft
Chuck Thacker

SEE YOU 1/10/77 OR SOONER.



DRAFT

Xerox Wire Functional Specification

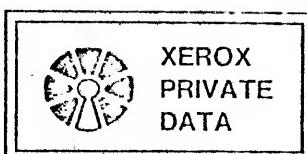
21 December 1976

1.0 OIS Communication Overview

This section appears with revisions in each of the documents produced by SDD Communication Systems. Its purpose is to reference other documents regarding Xerox Office Information Systems (OIS) communication and to provide context for this, the document in which it is contained.

1.1 The OIS Communication Environment

OIS is based on communicating digital processors called *system elements* or *hosts* used in a variety of configurations. Hosts communicate both for transmitting external information among OIS customers and for economic sharing of internal OIS resources. Existing office systems have hosts less numerous than copiers and less communicative than telecopiers. However, Xerox's asymptotic OIS, OIS in ~~is~~ eventual full development, has hosts more numerous than typewriters and more communicative than telephones. The special high-density frequent-use communication requirements of OIS have led Xerox to develop advanced packet communication protocols and devices.



OIS hosts include those configured as:

*word processing work stations,
central shared file stations,
printing stations,
image input-output stations, and
gateway stations.*

DWP/A

An OIS can begin as a single non-communicating work station which is later equipped to communicate with other work stations in the same location or work stations remotely located. A standalone copier can begin an OIS and later be made to communicate with others of its kind or to join an existing population of work stations to provide image input-output and printing facilities. Facilities for handling larger files, for remote communication, and for interconnection with non-OIS equipment can be incrementally centralized in shared hosts added as justified by the economics of system growth.

ADAM

1.2 The OIS Protocol

Various activities often associated with communication can usefully be arranged on the following major levels:

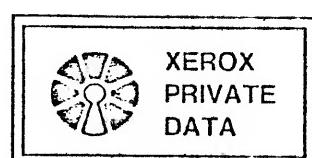
static formats: files, records, documents, forms, images.

dynamic formats: device control and file exchange.

transport protocols: media, processor, and application independent.

digital transmission: signalling and line control.

The OIS Protocol is set of packet transport protocols used uniformly across the variety of communication media, digital processors, and office applications, all of which may vary in OIS from installation to installation and from time to time.

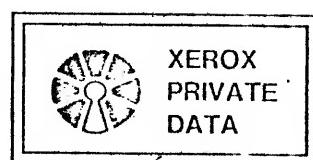


The OIS Protocol is based on digital transmission systems like those provided by the Xerox Wire, AT&T's Dataphone and Digital Dataphone Service, SBS's digital satellite channels, and Telenet's packet network. It is assumed that packets carried through such systems are subject to:

? ↘

*size limitations (~limit 1024 to 16384 bits),
propagation, queueing, and routing delays (~delay 1 to 1000 ms),
duplication (due to retransmission, rerouting, and lost acks),
reordering (due to retransmission and adaptive routing),
undetected damage (~damage 1 error in 10 to the 3rd to 12th bits),
unannounced loss (~loss 1 packet per 10 to 1,000,000),
misrouting (due to internal malfunction),
unauthorized perusal (surveillance), and
counterfeiting (sabotage).*

The OIS Protocol is based on the definition of a media, processor, and application independent OIS Protocol *packet*. Beneath the OIS Protocol are a set of formats and procedures for *encapsulating* and *decapsulating* OIS Protocol packets for transmission through each of the transmission systems employed. OIS packets are routed from source address to destination address, potentially through a variety of packet transmission systems, each encapsulating and decapsulating in its own media-dependent way. The OIS Protocol specifies how various end-to-end communication functions are accomplished using OIS Protocol packets independent of subsequent encapsulation and decapsulation.



Transport functions provided by facilities implementing the OIS Protocol include:

*naming and addressing and routing,
congestion control,
flow control,
error detection,
retransmission,
duplicate suppression,
sequencing, and
packetizing.*

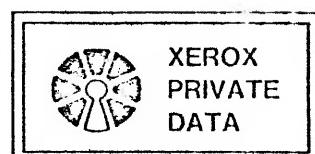
Unlike IBM's Systems Network Architecture (SNA), the OIS Protocol is based on distributed many-to-many communication as required by incrementally grown and increasingly interconnected office systems rather than hierarchical mainframe-centered data processing systems. *TAKE THAT.*

1.3 The Xerox Wire

The high density of frequently communicating hosts in the asymptotic OIS requires reliable and inexpensive local high-rate packet communication as provided by the Xerox Wire. The Xerox Wire is used for local packet transmission, underlying the OIS Protocol much as IBM's Synchronous Data Link Control (SDLC) underlies its SNA.

The principal components of an Xerox Wire are:

*wires (coaxial cable, connectors, and terminators),
taps (non-intrusive pressure taps and tees),
transceivers (at the tap, high-impedance when off),
interface cables (power and serial data),
interfaces (digital hardware, microcode, and Pilot drivers), and
repeaters (for active branching, boosting, and isolating wires).*



The topology of an Xerox Wire is that of a meandering and branching line. There is no central communication controller as might be found in a local communication system based on a digital PABX or loop (*a la* SDLC). The communication facility is the passive and therefore reliable and inexpensive coaxial cable which can be installed once or incrementally, as required. As new hosts are added, they tap into the Wire at its nearest point without disruption of communication service among other hosts.

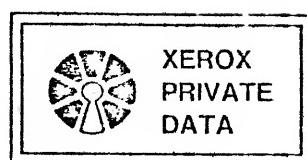
The Xerox Wire carries packets from any of 128 hosts to any other at a peak rate of 10 megabits per second over a repeaterless kilometer of coaxial cable. Applications and resource sharing are thus provided high data rates and rapid interaction among numerous and widely separated hosts in a campus.

1.4 Communication Using the OIS Operating System

Application programs running as processes under the OIS Operating System, Pilot, use OIS communication facilities via four grades of service, depending on requirements for generality and efficiency. These ~~grades~~ of service are offered in the following levels:

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- raw packet mode (routing packets unreliable to/from sockets),*
 - reliable packet mode (retransmission, flow control),*
 - packet stream mode (sequencing),*
 - byte stream mode (packetizing), and*
 - file transfer mode (file naming, typing, and exchange).*
- ?

The OIS Protocol is so organized that Pilot's grades of communication service are implemented in levels, one upon the other.



1.5 OIS Gateways

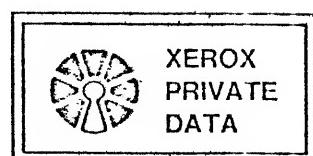
An OIS *campus* is a building or collection of adjacent buildings occupied by a number of hosts serving an OIS customer. OIS communication is of two kinds: *intracampus* and *intercampus*. Intracampus communication is through Xerox's proprietary high-rate packet communication system, the Xerox Wire. Intercampus communication uses common carrier data transmission facilities subject to FCC regulation and tariffs.

While the unique communication requirements of OIS demand the innovation of the Xerox Wire and the OIS Protocol, OIS must interconnect with and through numerous incompatible communication systems. Such interconnection is achieved, not by burdening each and every communication function with the requirement for direct compatibility with a number of non-OIS devices, but by capturing the effects of incompatibilities in *gateways*.

There are two kinds of incompatibility in OIS communication, *media incompatibility* and *protocol incompatibility*. The first, media incompatibility, arises from the use of packet communication media other than the Xerox Wire, say for example in intercampus OIS Protocol communication using AT&T's Dataphone or DDS and IBM's Bisync or SDLC. The second kind of incompatibility, protocol incompatibility, arises from communication with non-OIS systems, say for example with a Xerox 800 CETS or an IBM CMC/ST. Both kinds of incompatibility are captured in an OIS gateway, either a media gateway or a protocol gateway.

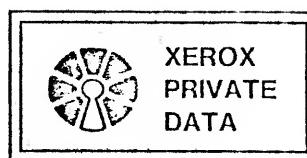
PORTOLA ↑ ↑ MAXC

Gateways need not occupy an entire host, but may appear in the same host as using application software or in a host providing other shared resources. For example, gateway modules may be included in a work station or, as economics dictate, in a shared file station or in a dedicated gateway station performing one or more gateway functions. An application using a gateway function is not written to depend on the manner in which gateway functions are distributed so that, for example, without changing application software, an OIS can grow from a single host OIS with coresident application and gateway functions to a multihost OIS with work stations and dedicated



gateway hosts joined through an Xerox Wire.

Intercampus communication is conducted among OIS hosts though a variety of common carrier facilities. The choice of a facility depends on the volume, frequency, and dispersion of communications. As lower-cost higher-rate modemless digital transmission facilities become available from AT&T, SBS, and others (generally at 50 kilobits per second and up), they are employed to carry higher volumes of imaginal data. As packet-switched facilities become available from AT&T, Telenet, and others, they are employed to carry higher dispersions of low-volume office communication.



MESA

USING PROCESS

XEROX WIRE
BOB METCALFE
7 DEC 76

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PILOT
MESA

SOCKET

PILOT MESA OIS PROTOCOL

ROUTER

PILOT
MESA

DRIVER

XEROX WIRE
PROCESSOR INTERFACE

D*
MICROCODE

MICROTASKS

HARDWARE

INTERFACE CABLE

TRANSCEIVER

XEROX WIRE
TRANSMISSION
DEVICES

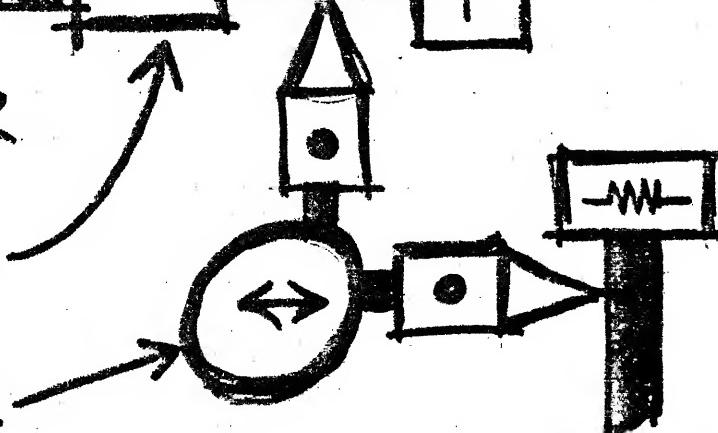
TAP



TERMINATOR

CONNECTOR

REPEATER



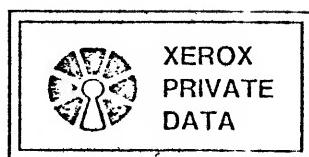
BIG BLOCK DIAGRAM

2.0 Xerox Wire Block Diagram Description

First, a look at the major pieces of a host's Xerox Wire communication facility as shown in the block diagram on the previous page and description below.

The OIS Protocol and Pilot Mesa. An OIS system element is called a *host* because it provides an environment for OIS *processes* running under the OIS Operating System, Pilot. Such processes are programmed in Mesa and use communication facilities provided by Pilot according to the OIS Protocol. Hosts are connected through varying packet transmission systems called *networks*. Using processes communicate either themselves or through a surrogate process by transmitting and receiving OIS Protocol packets via *sockets*. Sockets are Mesa data structures at which packets can be queued for transmission or queued upon receipt and between which packets move. Packets are *routed* when either they are transmitted from a socket or arrive at a host from a network to which it is connected. The router in each host determines by examining a packet's destination address whether the packet should be delivered to one of the sockets in the current host or forwarded through some network toward the host containing the specified destination socket. This routing is performed on packets whose format is specified by the media, processor, and application independent OIS Protocol.

Pilot Mesa Xerox Wire Driver. Once it has been determined by the router that a packet requires transmission through a certain network, that packet must be *encapsulated* for media-dependent transmission and later *decapsulated* for handling once again by the router in the specified next host's router. The Xerox Wire's driver is a set of Mesa programs and processes in Pilot which perform capsulation and schedule the allocation of packet buffers for transmission and receipt of Xerox Wire packets. The driver is both processor and media dependent being particularized to a given hardware implementation of the OIS processor architecture and to the Xerox Wire; it presents, however, a media, processor, and application independent interface to Pilot programs implementing the OIS Protocol.



Processor Dependent Xerox Wire Microtasks. Between the Mesa modules of the Xerox Wire driver and interface hardware are microprograms and associated hardware-scheduled tasks for performing low-level device control. These microprograms and tasks perform packet buffer queueing, data transfers between hardware buffers and main memory buffers, and retransmission control.

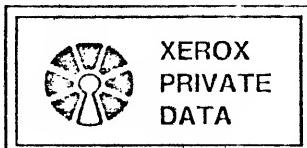
Xerox Wire Processor Interface Hardware. The Xerox Wire processor interface can be divided into two sections, one for controlling the transmission of packets and the other for controlling receipt. A first-in-first-out buffer is provided in each to compensate for main memory latency during packet-synchronous Xerox Wire transfers. Each section contains a shift register to provide for the (de)serialization of data between the processor's 16-bit data paths and the Xerox Wire's bit-serial packet transmissions. Digital circuits for phase encoding and decoding are provided along with CRC computation, retransmission countdown, and (possibly) address recognition.

Xerox Wire Interface Cable. The processor interface hardware controls the processor-independent Xerox Wire transceiver bit-serially through its interface cable. The transceiver ~~is~~ also powered through the interface cable.

is

Xerox Wire Transceivers. The Xerox Wire transceiver is a device for converting between the logic levels of the processor interface and the carefully generated and received transmission line signals carried through the Xerox Wire's meandering coaxial cable. The transceiver is very high impedance unless powered and turned on by the processor interface. The transceiver is never on for more than one half of a bit time and contains protection circuits to guard against the very undesirable wire-wide communication failure.

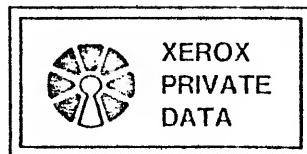
Xerox Wire Taps. The tap is a minimally intrusive mechanical device for connecting a transceiver through a short stub to the conductors of the Xerox Wire's coaxial cable. The tap must make installation and removal of hosts convenient and reliable without disruption of communication during installation.



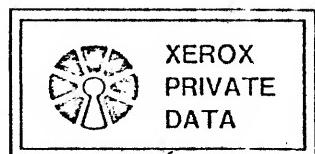
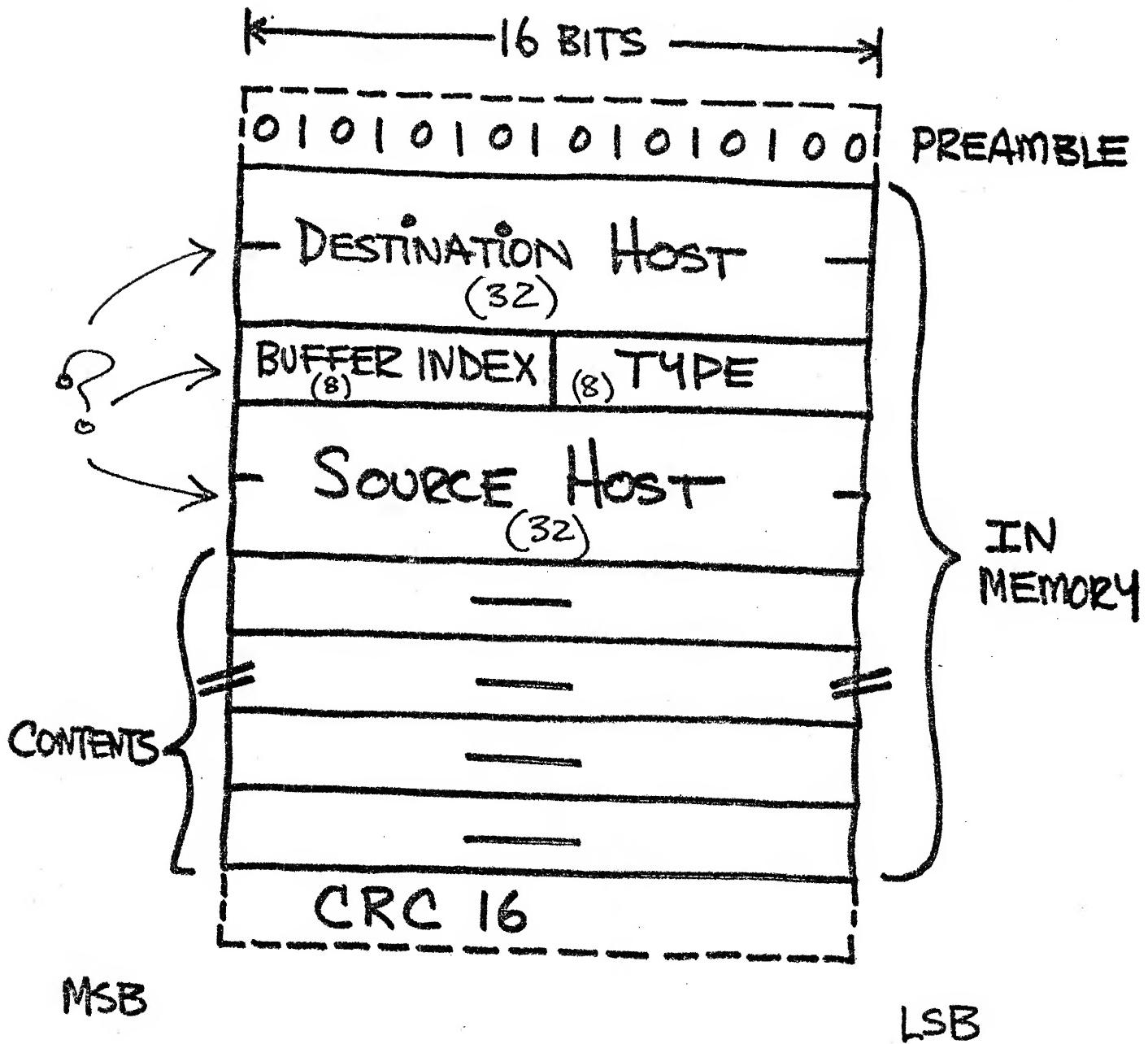
The Xerox Wire Wire. The Xerox Wire Wire is coaxial cable chosen for signal protection and ease of taping.

Xerox Wire Connectors. Lengths of the Xerox Wire are divided to make installation easier and to provide points for problem isolation. At each end of a stretch of cable is a female connector. Repeaterless lengths of Xerox Wire are concatenated with male-male connectors joining the female connectors on the end of each. At the extreme ends of a Xerox Wire, where no further extension is required, a male terminator is attached so that signal reflections will not occur. For observing packet transmissions during maintenance, a male-male tee is required.

Xerox Wire Repeaters. Between terminated segments of the Xerox Wire a repeater may be placed to carry packets between them. The repeater serves to boost signals, isolate segments, and branch.



Xerox Wire Packet Format

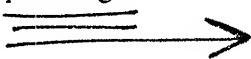


3.0 Xerox Wire Capsulation and Packet Format

Packet bits are transmitted from main memory, word by word, from most significant bit to least (left to right), and in order of increasing word addresses (top to bottom).

3.1 Preamble

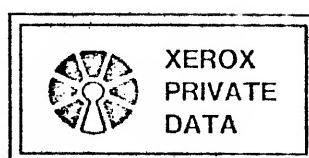
The preamble is not seen by software on either transmission or receipt. Its length, 16 bits, is calculated in the section below on the coaxial cable used for the Xerox Wire. The preamble is prefixed by microcode and used for packet synchronization by receiving hardware during cable precharge.



3.2 Destination Host Address

A host copies the bits of a passing Xerox Wire packet into its main memory when the host's own host address matches that in the packet's destination host address field, or when the packet's destination host address field indicates that it is a *broadcast* packet, or when the host's Xerox Wire interface has been set *promiscuous*.

Each OIS system element is assigned a 32-bit unique serial number at time of manufacture. There are two plans for assigning Xerox Wire host addresses. One plan simply uses the unique 32-bit serial number. The other uses a derived 8-bit host number. The first is better if destination address filtering can be done economically on 32 bits in hardware or in microcode. Otherwise, to avoid unacceptable field maintenance of unique host numbers on Xerox Wires, a simple protocol need be performed by hosts on a Xerox Wire to assure unique 8-bit host addresses for efficient destination address filtering in hardware or micocode. 32-bit host addresses are assumed for now.



A zero destination host address is illegal and indicates an error. An all ones destination host address indicates a *broadcast* packet to be accepted for software filtering by all hosts.

It is possible for software to suspend destination address filtering entirely for multiple address recognition and network surveys for billing and maintenance. When the destination host address is being ignored under this function, the host is said to be *promiscuous*.

3.3 Packet Buffer Dispatch Index

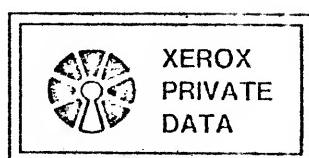


The packet buffer dispatch index is used by a receiving host to select the head of a packet buffer queue (most usefully containing only one packet buffer) so that the packet can be directed on the fly to its intended place in main memory. Presumably the source of a packet containing a non-zero buffer dispatch index has previously been sent this index by the receiving host. The zeroth entry in the buffer dispatch table contains a queue of packet buffers for normal packet receipt. This dispatch mechanism is somewhat redundant with virtual memory mapping which could move a packet to its intended location in virtual memory with a simple mapping operation rather than the copy which this mechanism is intended to avoid.

Buffer dispatch indices are a resource of the Pilot operating system allocated to communicating processes.

3.4 Xerox Wire Packet Type

The Xerox Wire packet type is normally one indicating that the packet's contents are an encapsulated OIS Protocol packet. A value of zero here is illegal and indicates an error. Other types may yet be invented for various Xerox Wire specific protocols, either for very high performance applications or diagnosis.



3.5 Source Host Address

The source host address field is the same size as the destination host address field. This field must always contain the host address of the host on the immediate Xerox Wire which originated transmission of the packet even though the packet may actually have been generated by some remote host using the last as a gateway. The source address is ignored by hardware and microcode under normal circumstances. A zero or all ones value here is illegal and indicates an error.

3.6 Contents and Length

The length of a Xerox Wire packet is not transmitted with it. The length is deduced by a receiver from the packet's length of transmission which must be an integral number of 16-bit words after preamble packet synchronization. The contents are transparent, meaning any bit combinations are legal and will not disrupt Xerox Wire communication. Aside from the limitations imposed by protocol, the actual length of a Xerox Wire packet, exclusive of preamble and CRC, can range between 5 and 65,535 16-bit words.

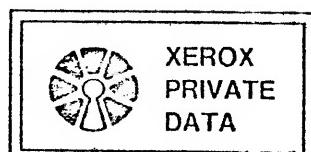
3.7 Cyclic Redundancy Check



The CRC is computed in hardware after packet data has entered the parity checked data paths of the processor so that transmitted data is continuously subject to some error control. A standard 16-bit CCITT CRC is used for ease of computing in hardware and good burst error protection.

4.0 Xerox Wire Mesa Control and Microtasks

Pilot Mesa control of packet transmits and receives are entirely independent as are the operation of microcode and hardware. A packet can be transmitted from a host to



itself. Furthermore, packet buffers are queued so that successive packets can be transmitted and received one immediately after the other in time on the Xerox Wire.

4.1 Packet Buffer Queues

Packet buffers are kept on queues. There is 1 such queue for transmission on a Xerox Wire. There are up to 256 for reception on a Xerox Wire, as selected by the packet buffer dispatch index discussed above. Each packet buffer is itself a queue of packet buffer control blocks supporting gather read and scatter write.

Gather read and scatter write are provided for two reasons. First, to allow headers and control information to be merged with data without copying. And second, to allow buffers to be allocated with units smaller than the largest allowed packet size.

Queue: TYPE = POINTER TO RECORD [head: Item, tail: Item];
 Item: TYPE = POINTER TO RECORD [next: Item, data: UNSPECIFIED];

If q is a Queue and i is an Item on q then:

If q.head=NIL then q is empty.

If q.head#NIL then q.head is head Item and q.tail is tail Item.

If i.next=NIL then i is tail Item and q.tail is i.

If i.next#NIL then i.next is next Item on q.

Enqueue[q,i]; -- put Item i on tail of Queue q

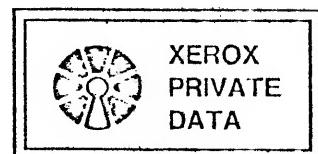
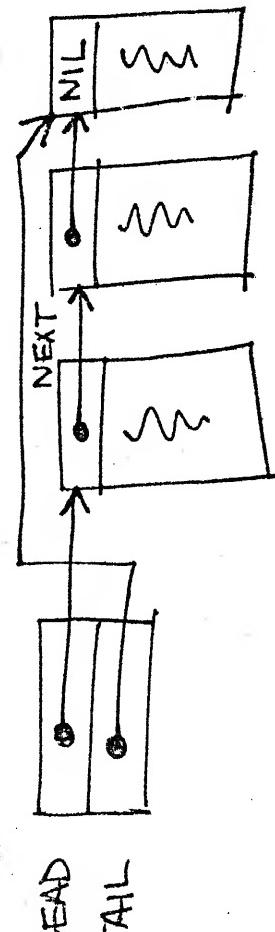
i←Dequeue[q]; -- get head Item or NIL from Queue q

PBQA is "Packet Buffer Queue Array".

PBQ is "Packet Buffer Queue", itself a Queue.

PBCB is "Packet Buffer Control Block".

PBB is "Packet Buffer Block".

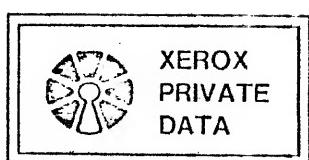


A Xerox Wire's PBQA is used for distributing input packets according to their packet buffer dispatch index so that they need not be copied to their intended place in memory. A PBQ is maintained by software for microtasks so that packets can be transmitted and received one right after the other with no gaps. A PB is a queue of blocks for gather read and scatter write. A PBCB points at a block of memory for packet words, indicates if the packet is continued, and holds transmission status.

```
PBQA: TYPE = POINTER TO ARRAY [0..255] OF PBQ;
PBQ: TYPE = POINTER TO RECORD [head: PB, tail: PB];
PB: TYPE = POINTER TO RECORD [next: PB, head: PBCB, tail: PBCB];
PBCB: TYPE = POINTER TO RECORD
  [
    next: PBCB, -- if NIL on receive, go to free queue for more
    length: INTEGER, -- total space in this block
    address: PBB,
    count: INTEGER, -- if negative, then last in packet
    status: PBStatus
  ];
PBB: TYPE = POINTER TO ARRAY [0..32767] OF WORD;
PBStatus: {outOK, inOK, badPBQ, loadOverflow, inOverflow, reset, ...};
```

4.2 Mesa Transmit Control

Each Xerox Wire has a transmit control block containing a word to point at a packet buffer queue, a word containing an initial load mask for collision randomizing, and a word containing an interrupt mask to be ORed into new wakeups waiting upon PBQ exhaustion or abnormal termination. Two commands are required, one to start transmission after new PBQ is prepared and one to reset during transmission. Two abnormal terminations are reset and load overflow. Transmission can be kept continuous safely either with atomic queue operations as described above or with idle checking after queue appends.



4.3 Mesa Receive Control

Where transmitting packets requires dealing with collisions and retransmissions, receiving packets requires dealing with address filtering and packet buffer dispatching.

When a passing packet is accepted through the address filter as described above, its packet buffer dispatch index must be examined on the fly and the appropriate packet buffer queue chosen from the packet buffer queue dispatch array. Next, the head packet buffer must be dequeued and its first packet buffer control block opened for disposal of arriving packet words. As successive control blocks are exhausted, the next ones must be found and setup on the fly until either the packet stops arriving or the packet buffer queue of control blocks is exhausted.

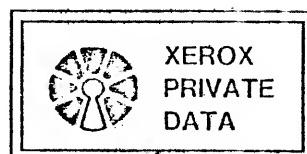
LATENCY? FIFO?

If the packet finishes, the length of the last segment of packet in its control block must be posted along with status indicating any errors in receipt. If the last control block of the packet buffer is exhausted, then, depending on an indicator in that block, either the receiver aborts with an overflow or a queue of unallocated control blocks is accessed to extend the current packet buffer. Thus, very long packets can be received, if desired, without preallocation of many control blocks to each packet buffer.

Receiver control requires a word pointing to the base of the packet buffer queue dispatch array, a two words containing the host address for address filtering (0 means promiscuous), and a word to contain the wakeup bit mask.

The two required commands are one to start the receiver and the other to reset it. Once again, queueing atomicity or careful idle detection and restart is required to keep the input continuously on.

It is required that the receiver be fast enough to receive immediately successive packets into prequeued input buffers.



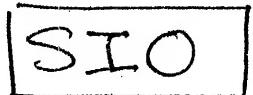
4.4 Mesa Features for the Xerox Wire

The following are features which are provided to Xerox Wire driving software by either Mesa bytecodes or through the Mesa runtimes.

4.4.1 Read Serial Number

Read 32-bit serial number for use as Xerox Wire host address.

4.4.2 Interface Commands



Start transmitter, start receiver, reset transmitter, reset receiver.

4.4.3 Task-Atomic Mesa Enqueue and Dequeue Bytecodes

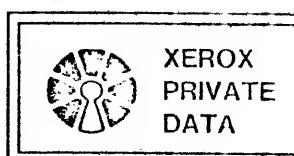


Perform Enqueue and Dequeue operations described above without doing a microcode task so that Xero Wire tasks can't run during pointer update and render pointers inconsistant.

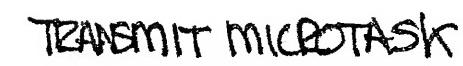
4.4.4 Checksum Mesa Bytecode



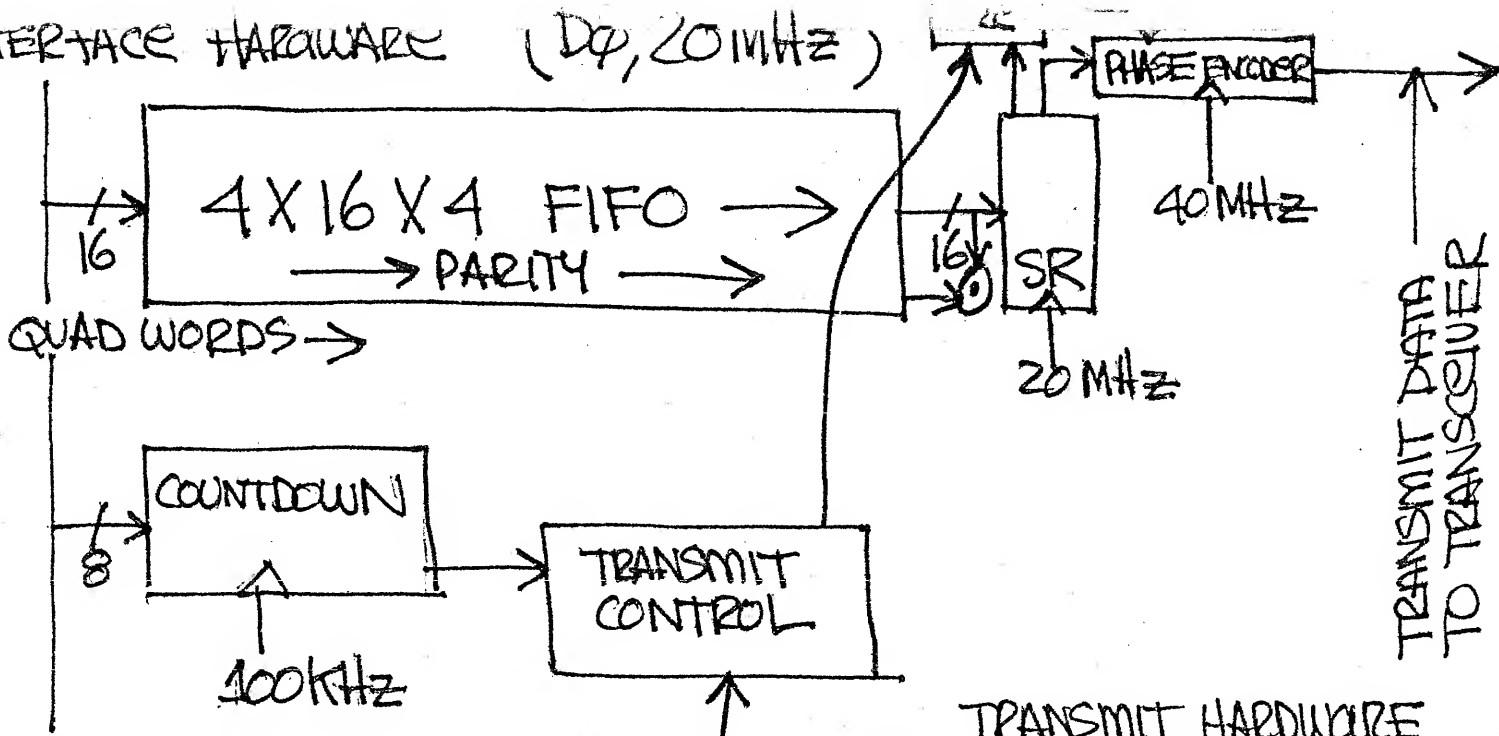
As part of "bit blit", compute 1's complement add and cycle checksum over specified block of memory words. This is really a requirement of the OIS Protocol, not the Xerox Wire.



XEDX WIRE INTERFACE HARDWARE (DQ, 20MHz)

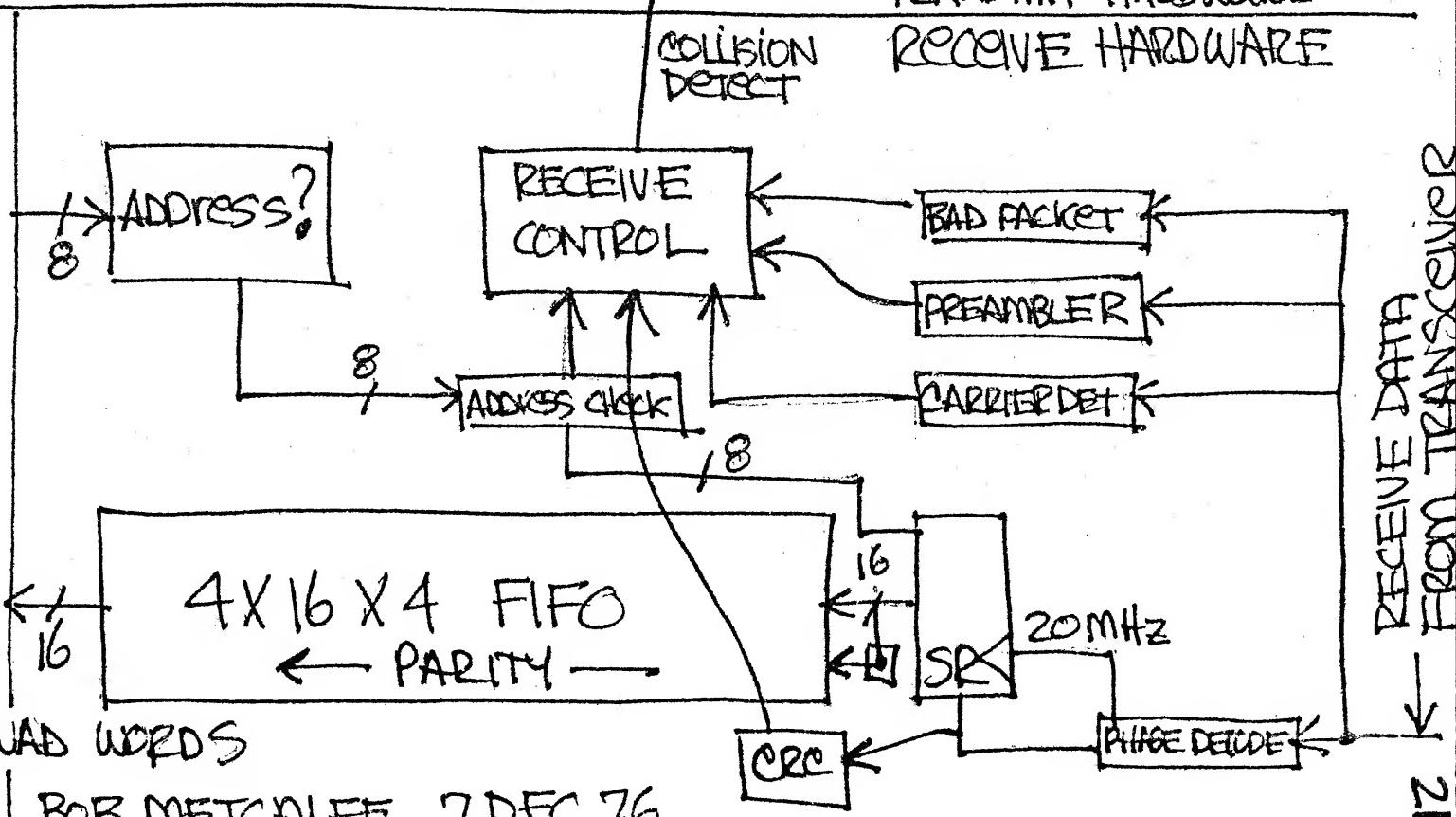


PB GET
LOAD INIT
COUNTDOWN SET
PREAMBLE
WORD GET
LOAD UPDATE
STATUS



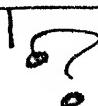
RECEIVE MICROTASK

ADDRESS GET
PB GET
WORD PUT
PACKET FILTER
STATUS



5.0 Xerox Wire Processor Interface

A system element is able to accommodate up to 4 Xerox Wire interfaces, the second sharing microcode with the first, and the third and fourth sharing a second copy of microcode. Each interface requires two microcode tasks, one for transmitting and one for receiving packets.



5.1 Phase Encoding and Decoding of Transmitted Serial Data

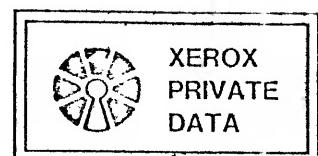
As packet bits are serialized and passed through the interface cable to the transceiver, they are phase encoded. In each bit cell, the first half of the bit cell contains the complement of the bit and the second half of the cell contains the bit itself. Thus, every bit cell has a transition and clock can be recovered by a receiver. This encoding produces 1.5 transitions per bit and keeps the transceiver off half the time during a packet transmission.

5.2 Collision Detection

Collision detection is accomplished for the transmitting section of the Xerox Wire interface by the receiving section. During phase decoding the arrival of phase transitions is used to determine whether the incoming signal is properly formed. If, after preamble synchronization is complete, the receiver detects bad phase encoding during a transmission, then the transmission is presumed to have suffered a collision.

5.3 Main Memory Latency Buffers

Because packet data arrives synchronously and because main memory has a non-zero latency, both for data transfers and buffer pointer manipulations, first-in-first-out



buffers are provided for both transmitting and receiving.

6.0 Xerox Wire Interface Cable and Transceiver

The Xerox Wire interface cable carries three signals and power. The signals are phase encoded serial data out, phase encoded serial data in, and interference detect in. The last of these is redundant with respect to phase encoding violation collision detection as described above.

The length of the interface cable is limited to 50 meters. Differential pairs are used in the interface cable.

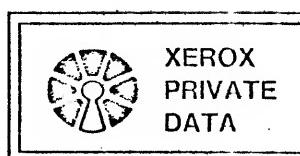
The processor interface will generate and expect to receive pulses of duration T or 2T according to the phase encoding rules. The transceiver is built to respond to T's between 25 and 500 nanoseconds supporting communication rates between 1 and 20 megabits per second. The expected operating point is at 10 megabits per second requiring T=50 and 2T=100 nanosecond pulses. Rise and fall times are 10 nanoseconds.

The transceiver requires 500 ma of 15 volts for powering its electronics.

The transceiver has the power and sensitivity to reach 127 other hosts on up to 1000 meters of repeaterless coaxial cable.

7.0 Xerox Wire Coaxial Cable, Taps, and Connectors

The Xerox Wire uses RG-11/U Type Foam Coaxial Cable, Belden Type 8233 having a dc resistance of 8.5 ohms per km and nominal capacitance of 56.8 picofarads per meter.



The connectors used are commercially available PL/259 females, male-male, male-male tees, and male terminators.

The taps used are commercially available Jerrold Electronics CATV CMT Pressure Taps.

The combined capacitance of tap and transceiver at each host is 10 picofarads.

The RC time constant of a km of Xerox Wire with 256 transceivers and taps depends only on the dc resistance ($1\text{km} \times 8.5 \text{ ohms/km}$) and nominal capacitance ($1000\text{m} \times 56.8\text{pf/m}$) of the coaxial cable, the cumulative capacitance of the transceiver and taps being negligible ($256 \times 10\text{pf}$). Thus the time constant for charging the cable is about .5 microseconds, or at 20 megabits per second, about 10 bit times. Thus the preamble of 16 bits is more than adequate (especially at 10 megabits per second) for the cable to charge during packet transmission and for the packet's bits to reach their full height for threshold receiving.

8.0 Xerox Wire Repeaters

Repeaters need not be placed until the number of transceivers on a Xerox Wire exceeds 128 or the length of the coaxial cable exceeds 1 km. Such repeaters are bidirectional packet repeaters and lock onto a packet for its duration. Packet pulses are retimed and preamble bits regenerated so that repeaters can safely be cascaded.

To what depth?

When a repeater detects a collision, it enforces a collision on all of its connected cables.

Repeaters are powered from normal 60 Hz 120 volt AC through the wall.

